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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/611,602	06/30/2003	Mike Hermes	MI22-2341	6154

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EXAMINER	
POMPEY, RON EVERETT	
ART UNIT	**PAPER NUMBER**
2812	

DATE MAILED: 02/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/611,602	HERMES, MIKE
	Examiner	Art Unit
	Ron E. Pompey	2812

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 December 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *44-49* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *44-49* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 44-49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dennison (5,292,677) in view of Arima (US 5,612,241).

Dennison discloses the steps of:

forming a plurality of conductive lines over a substrate having a memory array area and peripheral area outward of the memory array area;

removing insulative material, insulative cap (fig. 6B), over and exposing conductive material (26, fig.1) of conductive lines which are formed within a peripheral area outward of the memory array area, said exposing being a first-in-time exposure of conductive material of the conductive lines in the peripheral area after provision of said insulative material there over;

wherein the insulative material comprises a first insulative material, and further comprising prior to the removing of the first insulative material:

contemporaneously forming both capacitor container openings (41 fig. 2) within a second insulative material (32, fig. 2) over conductive lines within the memory array area, and contact openings (38, fig. 2) within the second insulative material over the conductive lines within the peripheral area;

forming a pair of capacitor electrode layers, storage node (42, fig. 6A) and cell plate (52, fig. 6A), and an intervening dielectric (50, fig. 6A) region therebetween within the capacitor container openings and the contact openings (col.12, lns. 11-52);

entirely removing the storage capacitor electrode layer within the capacitor container openings and not from within the capacitor container openings (fig. 6B); and

wherein the removing: of the first insulative material comprises using an etch chemistry effective to remove both the first insulative material (fig. 6B) and selected portions of the capacitor electrode layer over the memory array (col. 10, ln. 45 – col. 14, ln. 31).

3. Dennison discloses all the limitations of claims except for:

forming conductive material over the substrate comprising:

conductive plugs received over substrate node locations over which storage capacitors are to be formed within a memory array area; and

conductive material received over portions of some of the conductive lines within the peripheral area.

However:

a. Arima, discloses:

forming conductive material over the substrate comprising:

conductive plugs (15, fig. 3C) received over substrate node locations over which storage capacitors are to be formed within a memory array area; and

conductive material received over portions (16, fig. 3C) of some of the conductive lines within the peripheral area (col. 6, lns. 52-61).

Therefore it would be obvious to do for one of ordinary skill in the art, to combine Arima with Dennison, because the conductive plug will provide for better electrical contact to the memory device and peripheral devices.

Response to Arguments

Applicant's arguments filed 12-29-05, regarding claims 44-49, have been fully considered but they are not persuasive.

The applicant argues that "With respect to the motivation element to support a *prima facie* obviousness rejection, the present Action fails to provide any basis of motivation for the relied upon combination other than conclusory statements. ...It is unclear as to how the conductive plug recited in claim 44 can provide "better electric contact to memory device and peripheral devices"." To further clarify the statement "better electric contact to memory device and peripheral devices", the examiner would like to point to Arima, column 6, lines 1-20, which states, "..Therefore, even if the diffusion width of the source-drain regions 33a and 33b is made small, good connection with the interconnection layer 18 can be provided." . Therefore, Arima describes that better connection, or connection to a small area, can be achieved due to the forming of conductive plugs 15 and 16.

The applicant argues that, "Arima does not disclose or suggest the claim 44 recited entirely removing storage capacitor electrode layers and at least some of the conductive material received over conductive lines within a peripheral area to outwardly expose conductive portions of conductive lines." However, because the conductive

material disclosed by Arima is formed before the inter-dielectric layer therefore one of ordinary skill in the art would see that as Dennison clearly etches through the interlevel dielectric and other layers to the gate stack 26/24 figure 6B, with the combination of Arima (just for the formation of the conductive material over the substrate nodes and conductive lines over the gate stacks) that the conductive material 16, figure 3C of Arima would also be etched away to the gate electrode 31 in Arima as Dennison etches down to the gate electrode 26/24.

Conclusion

2. This is a Request for Continued Examination of the present application. All claims are drawn to the same invention claimed in the earlier application and could have been finally rejected on the grounds and art of record in the next Office action if they had been entered in the earlier application. Accordingly, **THIS ACTION IS MADE FINAL** even though it is a first action in this case. See MPEP § 706.07(b). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no, however, event will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ron E. Pompey whose telephone number is (571) 272-1680. The examiner can normally be reached on compressed.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael S. Lebentritt can be reached on (571) 272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ron Pompey
Ron Pompey
AU: 2812
February 6, 2006

MICHAEL LEBENTRITT
SUPERVISORY PATENT EXAMINER